AMENDMENTS

Please amend the application as indicated.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A phase lock loop circuit comprising a low power voltage-to-current converter ~~for use in a phase lock loop~~, comprising:

an input stage comprising:

a pair of differential signal input terminals operable to receive differential input signals from a charge pump;

first and second switching transistors each coupled to one of the pair of differential signal input terminals;

first and second complementary transistors coupled to the first and second switching transistor, respectively;

an output stage coupled to the first complementary transistors; and

a non-differential output terminal coupled to the output stage, where the output terminal is operable to transmit an output current signal as a function of voltages associated with the differential input signals.

2. (Currently Amended) The phase lock loop ~~voltage-to-current~~ converter of claim 1, where the input stage is a rail-to-rail input stage.

3. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 2, where the rail-to-rail input stage is a resistorless input stage.

4. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 1, where the voltage-to-current converter ~~current source~~ comprises a constant current source for the center frequency of the phase lock loop when the difference between the differential input signals is substantially zero.

5. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 1, wherein the output stage comprises a first output stage and a second output stage, the first output stage being coupled to the first complementary transistor and to the non-differential output terminal, the second output stage being coupled to the first output stage.

6. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 5, wherein the second output ~~input~~ stage comprises a bandgap reference circuit coupled to a bandgap reference signal and to a supply voltage.

7. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 6, wherein the bandgap reference signal is approximately 1.23 to 1.25 volts.

8. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 1, further comprising a biasing transistor coupled to a bias signal and to a supply voltage, wherein the biasing transistor is configured to generate a bias current for the input stage.

9. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 8, wherein a voltage associated with the biasing signal is approximately half of the supply voltage.

10. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 9, wherein the supply voltage is approximately 1.5 to 5 volts.

11. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 10, wherein the supply voltage is approximately 2.2 volts.

12. (Currently Amended) The phase lock loop ~~voltage-to-current~~ of claim 1, wherein the output stage is operable to provide substantially constant current sources for the center frequency of a phase lock loop resulting in an increase dynamic range of the voltage-to-current converter when the phase lock loop is locked and a voltage difference between the input signals is substantially zero.

13. (Currently Amended) The ~~A~~ phase lock loop circuit of claim 1, further comprising a phase and frequency detector coupled with a charge pump, a voltage controlled oscillator comprising the voltage-to-current converter and a current controlled

oscillator ~~of claim 1~~, and a loop filter coupled with the charge pump, the voltage controlled oscillator ~~to current converter~~ being coupled to the loop filter and to ~~with a current controlled oscillator that is coupled with~~ the phase and frequency detector.

14. (Original) The phase lock loop circuit of claim 13, further comprising a frequency divider coupled between the current controlled oscillator and the phase and frequency detector.

15. (Original) The phase lock loop circuit of claim 13, wherein the phase lock loop including the voltage-to-current converter does not have a dominant pole to degrade the phase lock loop stability.